

# Micrium

Empowering Embedded Systems

## μC/OS-II

and the  
Renesas M16C Processors

### Application Note

AN-1019

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Micrium provides high-quality embedded software components in the industry by way of engineer-friendly source code, unsurpassed documentation, and customer support. The company's world-renowned real-time operating system, the Micrium **μC/OS-II**, features the highest-quality source code available for today's embedded market. Micrium delivers to the embedded marketplace a full portfolio of embedded software components that complement **μC/OS-II**. A TCP/IP stack, USB stack, CAN stack, File System (FS), Graphical User Interface (GUI), as well as many other high quality embedded components. Micrium's products consistently shorten time-to-market throughout all product development cycles. For additional information on Micrium, please visit [www.micrium.com](http://www.micrium.com).

## About μC/OS-II

Thank you for your interest in **μC/OS-II**. **μC/OS-II** is a preemptive, real-time, multitasking kernel. **μC/OS-II** has been ported to over 45 different CPU architectures and now, has been ported to the Renesas M16C CPU.

**μC/OS-II** is small yet provides all the services you would expect from an RTOS: task management, time and timer management, semaphore and mutex, message mailboxes and queues, event flags and much more.

You will find that **μC/OS-II** delivers on all your expectations and you will be pleased by its ease of use.

## Licensing

**μC/OS-II** is provided in source form for **FREE** evaluation, for educational use or for peaceful research. If you plan on using **μC/OS-II** in a commercial product you need to contact Micrium to properly license its use in your product. We provide ALL the source code with this application note for your convenience and to help you experience **μC/OS-II**. The fact that the source is provided **DOES NOT** mean that you can use it without paying a licensing fee. Please help us continue to provide the Embedded community with the finest software available. Your honesty is greatly appreciated.

## Manual Version

If you find any errors in this document, please inform us and we will make the appropriate corrections for future releases.

Version	Date	By	Description
V.1.00	2007/02/26	BAN	Initial version.

## Software Versions

This document may or may not have been downloaded as part of an executable file containing the code described herein plus (possibly) additional application or board support code. If so, then the versions of the Micrium software modules in the table below would be probably included. In either case, the software port described in this document uses the module versions in the table below

Module	Version	Comment
μC/OS-II	V2.83	

## Document Conventions

### Numbers and Number Bases

- Hexadecimal numbers are preceded by the “0x” prefix and displayed in a monospaced font. Example: `0xFF886633`.
- Binary numbers are followed by the suffix “b”; for longer numbers, groups of four digits are separated with a space. These are also displayed in a monospaced font. Example: `0101 1010 0011 1100b`.
- Other numbers in the document are decimal. These are displayed in the proportional font prevailing where the number is used.

### Typographical Conventions

- Hexadecimal and binary numbers are displayed in a monospaced font.
- Code excerpts, variable names, and function names are displayed in a monospaced font. Functions names are always followed by empty parentheses (e.g., `OS_Start()`). Array names are always followed by empty square brackets (e.g., `BSP_Vector_Array[ ]`).
- File and directory names are always displayed in an italicized serif font. Example: */Micrium/Software/uCOS-II/Source/*.
- A bold style may be layered on any of the preceding conventions—or in ordinary text—to more strongly emphasize a particular detail.
- Any other text is displayed in a sans-serif font.

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# 1. Introduction

This document describes the official Micrium port for  $\mu$ C/OS-II to the Renesas M16C/R8C family of processors. Figure 1-1 diagrams the relationship between your application,  $\mu$ C/OS-II, the port code and the BSP (Board Support Package). Relevant sections of this application note are labeled on the figure

If this appnote was downloaded in a packaged executable zip file, then it should have been found in the directory `/Micrium/Appnotes/AN1xxx-RTOS/AN1019-uCOS-II-Renesas-M16C` and the code files referred to herein are located in the directory structure displayed in Section 3.01; these files are also described in Section 3.01. The M16C has been ported on both the IAR and HEW tools.

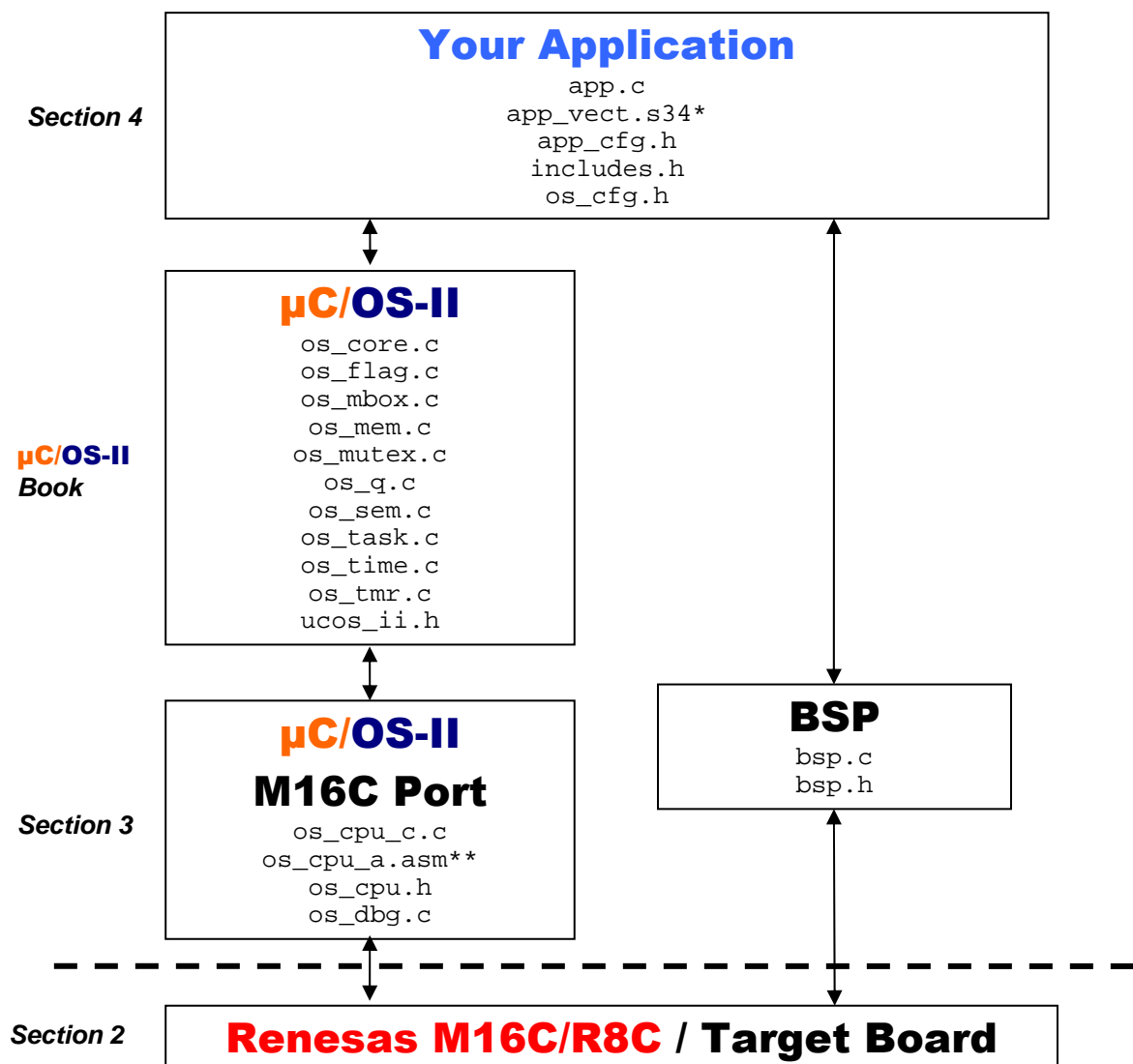


Figure 1-1. Code Block Diagram.

\*For the HEW port, this file is named `_linker.inc` and is part of the BSP.

\*\*For the HEW port, this file is named `os_cpu_a.a30`.

## 2. The M16C/R8C Programmer's Model

The visible CPU registers in a M16C or R8C processor are shown in Figure 2-2. Besides the `PC` (Program Counter) and `INTB` (Interrupt Table) registers, which are each 20 bits wide, these registers are all 16-bit registers. The registers are as follows:

- **Data Registers: `R0`, `R1`, `R2`, `R3`.** These are mainly used for transfers and arithmetic/logic operations. The `R0` and `R1` registers can each be separated into two 8-bit registers. 32-bit registers can be formed by combining `R2` and `R0` or by combining `R3` and `R1`; these registers are referred to as `R2R0` and `R3R1`.
- **Address Registers: `A0`, `A1`.** These are used primarily for address register indirect addressing and address register relative addressing, in addition to being used for transfers and arithmetic/logic operations. `A1` and `A0` may be combined and used as a single 32-bit register, `A1A0`.
- **Frame Base Register, `FB`.**
- **Interrupt Table Register, `INTB`.** This register contains the start address of the relocatable interrupt vector table.
- **Program Counter, `PC`.** This register indicates the address of the next instruction to be executed.
- **Static Base Register, `SB`.**
- **Flag Register, `FLG`.** This register indicates the CPU states. The bits of this register are described in Figure 2-3.
- **Stack Pointers, `USP` and `ISP`.** These are the stack pointers for the two processor modes, user and interrupt. The μC/OS-II M16C port requires the processor to be initialized in interrupt mode, and only the `ISP` will be used.

The data registers, address registers, and frame base register comprise a register bank, of which two are present on the processor. This second bank of register could be used to provide fast context switch (when an interrupt occurs, for instance); however the μC/OS-II port does not use the second bank of registers.

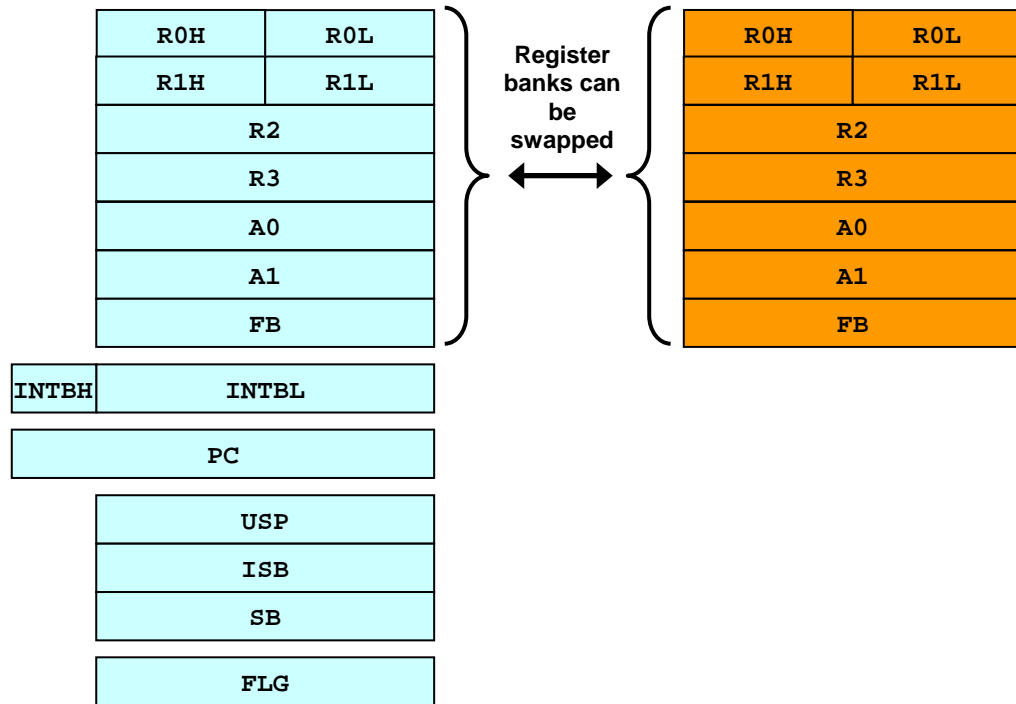


Figure 2-2. M16C Registers

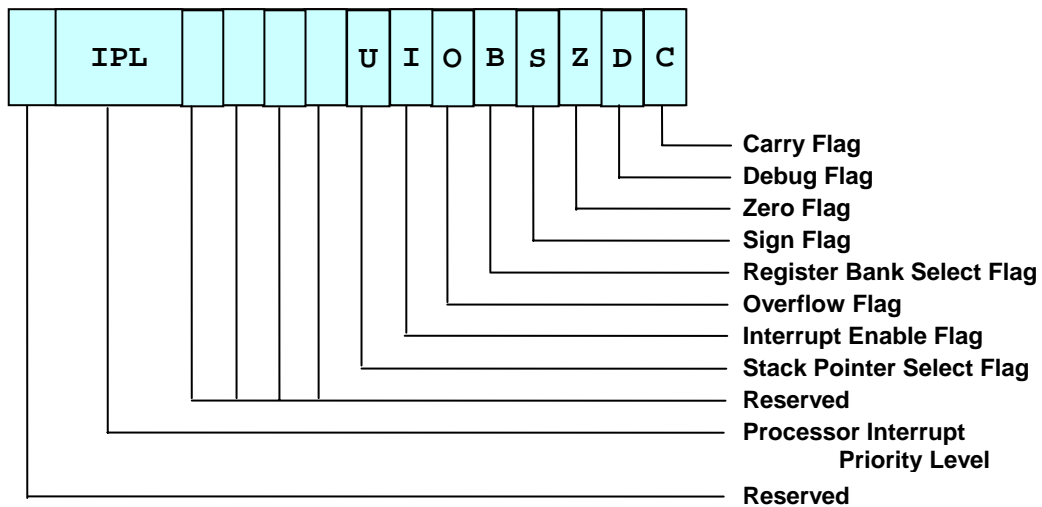


Figure 2-3. M16C FLAG Register

### 3. μC/OS-II Port for the M16C/R8C

Two toolchains were used to compile the M16C port. The first is IAR EW (Embedded Workbench) for M16C/R8C processors, V3.21A. The second is Renesas's HEW (High-Performance Embedded Workshop) V4.00 using the NC30WA compiler. Though code for these tools are compatible, meaning that a project compilable under one can be adapted for the other, the expectations of the tools are not identical. Table 3-1 summarizes the differences between the assembly code for the projects created for these toolchains. Differences between the tools will also be discussed at appropriate points in the appnote, where some specific difference is encountered.

The project was tested on a Renesas SKP16C62P evaluation board, as shown in Figure 3-1. The port could also be used on other M16C and R8C processors with no change to the μC/OS-II port; however, a suitable BSP would need to be provided. This would initialize the timer used for the μC/OS-II tick interrupt in addition to initializing the hardware peripherals used by the application (such as GPIO pins or a UART).

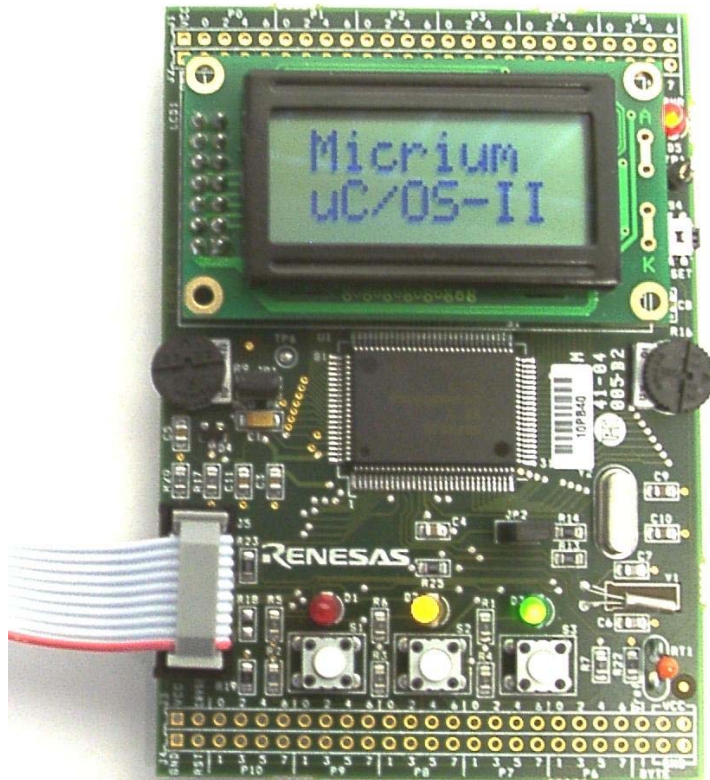


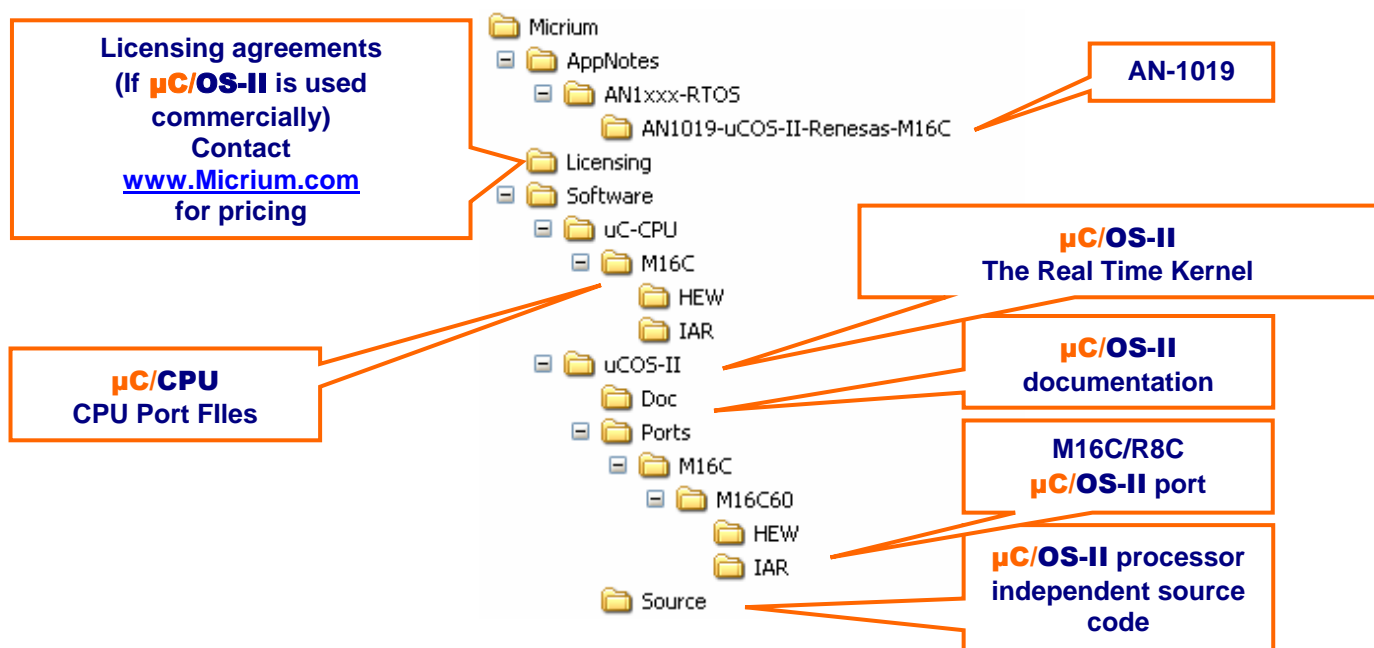
Figure 3-1. Renesas SKP16C62P Evaluation Board

Item	IAR	HEW
Extern directive	EXTERN	.glb
Import directive	PUBLIC	.glb
Declare 32-bit constant	DC32	.lword
End of file	END	.END
Section directive (for function)	Functions are preceded by:  .EVEN FncName: <function>  (The name of the function is externed at the beginning of the assembly file.)	Functions are be preceded by:  .SECTION program .GLB _FncName  _FncName: <function>
Variables	As used in C	C name preceded by underscore

**Table 3-1. Differences between IAR and HEW in Port's Assembly Code**

## 3.01 Directories and Files

If this file, *AN-1019*, were downloaded as part of an executable zip file, then the code files referred to herein are located in the directory structure shown in Figure 3-2. Additional application or BSP code may have been included in that executable zip file that is not listed in Figure 3-2.



**Figure 3-2, Directory Structure**

The source code for the **μC/OS-II** port with the IAR toolchain is found in the following directory:

`\Micrium\Software\uCOS-II\M16C\M16C60\IAR`

Similarly, for the HEW toolchain using the NC30WA compiler, the **μC/OS-II** port is in

`\Micrium\Software\uCOS-II\M16C\M16C60\HEW`

Each port consists of four files:

- *os\_cpu.h* contains processor- and implementation-specific `#define` constants, macros, and typedefs.
- *os\_cpu\_a.asm* (named *os\_cpu\_a.a30* for the HEW port) contains five simple assembly language functions.
- *os\_cpu\_c.c* contains ten simple C-language functions, including the function that initializes the task stacks.
- *os\_dbg.c* was added in V2.62 of **μC/OS-II** to allow a kernel-aware debugger to extract information about **μC/OS-II** and its configuration.

Also included is the **μC/CPU** port; for the IAR toolchain, this is found in the directory

`\Micrium\Software\uC-CPU\M16C\IAR`

Similarly, for the HEW toolchain using the NC30WA compiler, the **μC/CPU** port is in

`\Micrium\Software\uC-CPU\M16C\HEW`

In both cases, the port consists of two files:

- *cpu.h* contains processor- and implementation-specific `#define` constants, macros, and typedefs. The application code should use these defines to create platform-independent source code.
- *cpu\_a.s34* (named *cpu\_a.a30* for the HEW port) includes functions, written in assembly language, for enabling and disabling interrupts and saving and restoring the CPU flags.

## 3.02 μC/OS-II Port: *os\_cpu.h*

### 3.02.01 Data Types

μC/OS-II is made compiler- and CPU-independent by defining in the port the data types used in the source code. These, shown in Listing 3-1, are the same for both the HEW and IAR toolchains.

```
typedef unsigned char  BOOLEAN;
typedef unsigned char  INT8U;
typedef signed   char  INT8S;
typedef unsigned int   INT16U;
typedef signed   int   INT16S;
typedef unsigned long  INT32U;
typedef signed   long  INT32S;
typedef float         FP32;
typedef double        FP64;

typedef unsigned int   OS_STK;
typedef INT16U         OS_CPU_SR;
```

**Listing 3-1. *os\_cpu.h*: Data Type Definitions**

### 3.02.02 Critical Sections

μC/OS-II, as with all real-time kernels, needs to disable interrupts in order to ensure critical sections are evaluated atomically. Macros are provided to disable and enable interrupts: `OS_ENTER_CRITICAL()` and `OS_EXIT_CRITICAL()`, respectively. μC/OS-II defines three ways to disable interrupts, but only one of these methods needs to be used. The preferred method is typically method number 3. Note that if critical method 3 is used, a local variable `cpu_sr` must be allocated and initialized to zero in the user code.

```
#if OS_CRITICAL_METHOD == 1
#define OS_ENTER_CRITICAL() asm("FCLR I")
#define OS_EXIT_CRITICAL()  asm("FSET I")
#endif

#if OS_CRITICAL_METHOD == 2
#define OS_ENTER_CRITICAL() asm("PUSHC FLG"); asm("FCLR I") /* (1) */
#define OS_EXIT_CRITICAL()  asm("POPC FLG")
#endif

#if OS_CRITICAL_METHOD == 3
#define OS_ENTER_CRITICAL() asm("STC FLG, $@", cpu_sr);asm("FCLR I")
#define OS_EXIT_CRITICAL()  asm("LDC $@, FLG", cpu_sr)
#endif
```

**Listing 3-2. *os\_cpu.h*: Critical Sections**

**Listing 3-2, Note 1:** Code is provided for critical method 2 for completeness only. This code will not work if data have been stored on the stack after entering the critical section, but have not been all removed when exiting the critical section.

### 3.02.03 Stack Growth

The stacks on the Renesas M16C/R8C grow from high memory to low memory; consequently, `OS_STK_GROWTH` is set to 1.

```
#define OS_STK_GROWTH 1
```

**Listing 3-3. *os\_cpu.h*: Stack Growth**

### 3.02.04 Task-Level Context Switch

Task-level context switches are performed when **μC/OS-II** invokes the macro `OS_TASK_SW()`. Because context-switching is processor specific, `OS_TASK_SW()` needs to execute assembly-language code. For the M16C/R8C port, a task switch is triggered using software interrupt 0. The task switch handler, `OSCtxSw()`, will need to be placed on vector 0.

```
#define OS_TASK_SW() asm("INT #0")
```

**Listing 3-4. *os\_cpu.h*: Context Switch**

### 3.02.05 Function Prototypes

The prototypes in Listing 3-5 are for function defined in *os\_cpu\_a.asm* (which is named *os\_cpu\_a.a30* for the HEW port).

```
void OScTxSw (void);
void OSIntCtxSw (void);
void OSStartHighRdy (void);
void OSTickISR (void);
```

**Listing 3-5. *os\_cpu.h*: Function Prototypes**

## 3.03 μC/OS-II Port: *os\_cpu\_c.c*

A **μC/OS-II** port requires that you write ten fairly simple C functions, as listed below. The functions whose names are written in bold are non-empty. However, any of the hooks may be configured to provide some functionality important for your application.

- **OSTaskStkInit()** is typically the only function that need be defined for a port. This function is discussed in the subsection 3.03.01.
- **OSInitHookBegin()** is called by **μC/OS-II**'s `OSInit()` at the very beginning of `OSInit()`, giving the opportunity to add additional port-specific initialization. In this case, the global variable `OSTmrCtr` (used by the `os_tmr.c` module) is initialized to 0.
- `OSInitHookEnd()`
- **OSTaskCreateHook()** is called by **μC/OS-II**'s `OSTaskCreate()` or `OSTaskCreateExt()` when a task is created. If **μC/OS-View** (which performs task profiling as run-time) is included as part of the build, the function `OSView_TaskCreateHook()` is called, initializing **μC/OS-View**'s data for that task.
- `OSTaskDelHook()`
- `OSTaskIdleHook()`
- `OSTaskStatHook()`
- **OSTaskSwHook()** is called when a context switch occurs. This function allows the code to measure the execution time of a task for instance. In this case, the **μC/OS-View** task switch hook, `OSView_TaskSwHook()`, is called, allowing **μC/OS-View** to do exactly that.
- `OSTCBInitHook()`
- **OSTimeTickHook()** is called at the beginning of `OSTimeTick()`. This function calls `OSView_TickHook()`. It also determines whether it is time to update the **μC/OS-II** timers; if it is time to update the timers, the timer task is signalled.

### 3.03.01 Task Stack Initialization: **OSTaskStkInit()**

The code in Listing 3-6 initializes the stack frame for the task being created. The task receives an additional argument, `p_arg`, which is assigned into a register when the task stack is created. Because the initial value of the CPU registers is largely unimportant, the initial values include some indication of the register name, which might be helpful for debugging and examining the stacks in RAM.

The task stack structure is shown in Figure 3-3. When a context switch occurs, the bottom eight stack entries will be returned to the CPU registers using a stack pop (`POP.M`) command. Because the upper two entries are returned to the CPU registers with a `REIT` command, and these are formatted in the manner expected by the processor architecture.

```

OS_STK *OSTaskStkInit (void (*task)(void *pd), void *pdata, OS_STK *ptos, INT16U opt)
{
  INT16U  *pstk16;
  INT16U  flag;

  flag      = 0x0040;                                /* (1) */
  pstk16    = (INT16U *)ptos;
  pstk16--;

  *pstk16-- = (flag      & 0x00FF)
              | (((INT32U)task >> 8) & 0x00000F00)
              | ((flag << 4) & 0xF000);
  *pstk16-- = (((INT32U)task) & 0x0000FFFF);

  *pstk16-- = (INT16U)0xFBFB;
  *pstk16-- = (INT16U)0x3B3B;
  *pstk16-- = (INT16U)0xA1A1;
  *pstk16-- = (INT16U)0xA0A0;
  *pstk16-- = (INT16U)0x3333;
  *pstk16-- = (INT32U)pdata >> 16L;
  *pstk16-- = (INT32U)pdata & 0x0000FFFFL;
  *pstk16   = (INT16U)0x0000;

  return ((OS_STK *)pstk16);                        /* (2) */
}

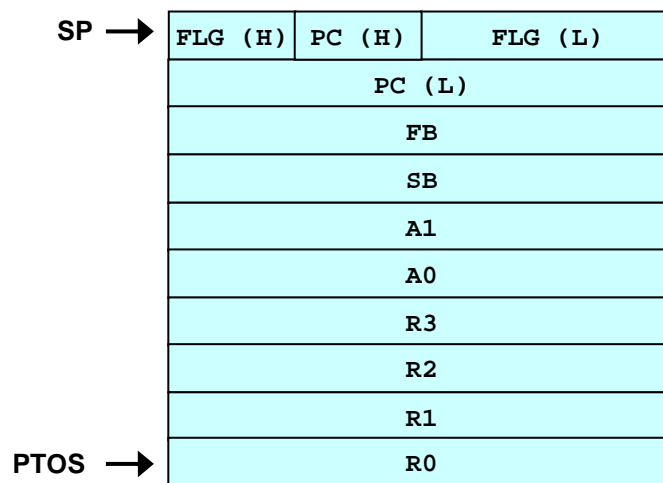
```

**Listing 3-6. *os\_cpu.c*: OSTaskStkInit()**

**Listing 3-6, Note 1:** The task stack is initialized so that interrupts are enabled the first time the task executes. If interrupts were not enabled, then no context switch could ever occur.

**Listing 3-6, Note 2:** The pointer to the top of the stack is returned.

### 3.03.02 M16C/R8C Stack Frame



**Figure 3-3. Task Stack Frame**

## 3.03 μC/OS-II Port: *os\_cpu\_a.asm*

A μC/OS-II port requires three fairly simple assembly-language function:

- `OSStartHighRdy()` is called by `OSStart()` to start running the highest-priority task.
- `OSCtxSw()` performs a task-level context switch.
- `OSIntCtxSw()` performs an interrupt-level context switch.

In addition, a fourth function, `OSTickISR()` is defined in *os\_cpu\_a.asm*. This function is the ISR for the μC/OS-II tick IRQ. The function `OSTickISR()` should be placed on the appropriate IRQ vector.

The assembly code shown in this chapter is for the IAR compiler. The HEW code differs only in the assembler directives used, such as those which specify the memory segment into which the code will be placed. Table 3-1 lists these difference; in addition, please consult *os\_cpu\_a.a30* in

`\Micrium\Software\uCOS-II\M16C\M16C60\HEW`

for a full listing of the HEW assembly source code.

### 3.03.01 Beginning Multitasking: `OSStartHighRdy()`

`OSStartHighRdy()` is called by `OSStart()` to start running the highest priority task that was created before calling `OSStart()`. `OSStart()` sets `OSTCBHighRdy` to point to the `OS_TCB` of the highest-priority task.

```

OSStartHighRdy:
  JSR          OSTaskSwHook                ; Note 1

  MOV.W       OSTCBHighRdy, A0            ; ISP = OSTCBHighRdy->OSTCBStkPtr
  LDC        [A0], ISP

  MOV.B       #01H, OSRunning             ; Note 2: OSRunning = TRUE
  POPM       R0,R1,R2,R3,A0,A1,SB,FB     ; Note 3

  REIT
```

**Listing 3-7. *os\_cpu\_a.asm*: `OSStartHighRdy()`**

**Listing 3-7, Note 1:** The task switch hook is called.

**Listing 3-7, Note 2:** Set `OSRunning` to `TRUE`.

**Listing 3-7, Note 3:** The data registers, address registers, stack base register, and frame base register are popped from the task stack into the CPU registers. The next two stack entries, which contain the `FLG` and `PC` registers will be popped with the `REIT` command.

## 3.03.02 Performing a Task-Level Context Switch: `OSCtxSw()`

When a task yields control of the CPU, the `OS_TASK_SW()` macro is invoked. For the M16C, this macro causes a interrupt, IRQ 0. The function `OSCtxSw()` should be placed on the IRQ 0 vector.

```

OSCtxSw:
    PUSHM    R0,R1,R2,R3,A0,A1,SB,FB    ; Note 1

    MOV.W    OSTCBCur, A0                ; Note 2: OSTCBCur->OSTCBStkPtr = SP
    STC      ISP, [A0]

    JSR      OSTaskSwHook                ; Note 3: OSTaskSwHook()

    MOV.W    OSTCBHighRdy, OSTCBCur     ; Note 4: OSTCBCur = OSTCBHighRdy

    MOV.W    OSPrioHighRdy, OSPrioCur   ;           OSPrioCur = OSPrioHighRdy

    MOV.W    OSTCBHighRdy, A0           ; Note 5: SP           = OSTCBHighRdy->OSTCBStkPtr
    LDC      [A0], ISP

    POPM     R0,R1,R2,R3,A0,A1,SB,FB    ; Note 6

    REIT
    
```

**Listing 3-8.** *os\_cpu\_a.asm*: `OSCtxSw()`

**Listing 3-8, Note 1:** The data registers, address registers, stack base register, and frame base register are saved on the previous task's stack (the stack of the task yielding the processor). The PC and FLG register were already placed on the stack when the interrupt occurred.

**Listing 3-8, Note 2:** The stack pointer is saved.

**Listing 3-8, Note 3:** The task switch hook function is invoked.

**Listing 3-8, Note 4:** `OSTCBCur` and `OSPrioCur` are assigned the proper values for the new task, which are currently `OSTCBHighRdy` and `OSPrioHighRdy`.

**Listing 3-8, Note 5:** The stack pointer is initialized.

**Listing 3-8, Note 6:** The processor registers are popped from the new task's stack. The PC and FLG registers will be popped from the stack with the `REIT` command.

### 3.03.03 Performing an Interrupt-Level Context Switch: OSIntCtxSw()

When an ISR completes, OSIntExit() is called to determine whether a more important task than the interrupt task needs to execute. If that is the case, OSIntExit() determines which task should run next and calls OSIntCtxSw(). The code for this function is identical to OSTxSw(), except that neither the registers nor the stack pointer need to be save on entry to the function.

```

OSIntCtxSw:
  JSR      OSTaskSwHook          ; Note 1: OSTaskSwHook()

  MOV.W   OSTCBHighRdy, OSTCBCur ; Note 2: OSTCBCur = OSTCBHighRdy

  MOV.W   OSPrioHighRdy, OSPrioCur ;      OSPrioCur = OSPrioHighRdy

  MOV.W   OSTCBHighRdy, A0      ; Note 3: SP      = OSTCBHighRdy->OSTCBStkPtr
  LDC     [A0], ISP

  POPM    R0,R1,R2,R3,A0,A1,SB,FB ; Note 4
  REIT
  
```

**Listing 3-9. *os\_cpu\_a.asm*: OSIntCtxSw()**

**Listing 3-9, Note 1:** The task switch hook function is invoked.

**Listing 3-9, Note 2:** OSTCBCur and OSPrioCur are assigned the proper values for the new task, which are currently OSTCBHighRdy and OSPrioHighRdy.

**Listing 3-9, Note 3:** The stack pointer is initialized.

**Listing 3-9, Note 4:** The processor registers are popped from the new task's stack. The PC and FLG registers will be popped from the stack with the REIT command.

### 3.03.04 Tick ISR: OSTickISR()

The μC/OS-II tick ISR, OSTickISR() is also included in *os\_cpu\_a.asm*. This function can be used on any M16C/R8C platform, as long as no further acknowledgement is required for the timer hardware (like resetting the timer counts, for instance). In any case, this function should serve as a template for any ISR for the M16C/R8C.

```

OSTickISR:
    PUSHM      R0,R1,R2,R3,A0,A1,SB,FB      ; Note 1: Save current task's registers
    INC.B      OSIntNesting                 ; Note 2: OSIntNesting++
    CMP.B      #1,OSIntNesting             ; Note 3: if (OSIntNesting == 1) {
    JNE        OSTickISR1
    MOV.W      OSTCBCur, A0                 ;           OSTCBCur->OSTCBStkPtr = SP
    STC        ISP, [A0]                   ;           }
OSTickISR1:
    JSR        OSTimeTick                   ; Note 4: OSTimeTick()
    JSR        OSIntExit                    ; Note 5: OSIntExit()
    POPM      R0,R1,R2,R3,A0,A1,SB,FB     ; Note 6: Restore current task's registers
    REIT
  
```

**Listing 3-10.** *os\_cpu\_a.asm*: OSTickISR()

**Listing 3-10, Note 1:** The current task's registers are saved.

**Listing 3-10, Note 2:** The interrupt nesting level is incrementing.

**Listing 3-10, Note 3:** If a task was interrupted, then the stack pointer is saved..

**Listing 3-10, Note 4:** OSTimeTick() is called to inform μC/OS-II of the interrupt.

**Listing 3-10, Note 5:** OSIntExit() is called to determine if a task with a higher priority than the one interrupted exists. If one does, then OSIntExit() never returns.

**Listing 3-10, Note 6:** The current task's registers are restored.

### 3.04 μC/OS-II Port: *os\_dbg.c*

This file was added in μC/OS-II V2.62 to allow a kernel-aware debugger to extract information about μC/OS-II and its configuration. If your debugger does not need this file, you may omit it in your build.

## 4. Interrupt Handling for the M16C/R8C

The M16C/R8C processors contain two vector tables. The **fixed vector table** is located at the highest addresses—from 0xFFFFDC to 0xFFFFF—contains software and hardware non-maskable interrupts. These are listed in Table 4-1. The **relocatable vector table** contains maskable peripheral-function interrupts and, as its name implies, does not need to be at a fixed location. The location of this table should be assigned to the INTB register in the processor startup code. The purpose of the vectors in the fixed vector table does not vary between different M16C/R8C processors; however, the purpose of the vectors in the relocatable vector table depends on the peripherals present on a particular chip. An example relocatable vector table is given in Table 4-2 for the M16C/62P processor.

Interrupt source	Vector Table Address
Undefined instruction	0xFFFFDC
Overflow	0xFFFFE0
BRK instruction	0xFFFFE4
Address match	0xFFFFE8
Single step	0xFFFFEC
Watchdog timer	0xFFFFF0
DBC	0xFFFFF4
NMI	0xFFFFF8
Reset	0xFFFFFC

**Table 4-1. R16C/R8C Fixed Vector Table**

Interrupt source	IRQ Number
BRK instruction	0
INT3	4
Timer B5	5
Timer B4; UART1 bus collision	6
Timer B3; UART0 bus collision	7
SI/O4, INT5	8
SI/O3, INT4	9
UAR2 bus collision	10
DMA0	11
DMA1	12
Key input interrupt	13
· · · ·	·
· · · ·	·
· · · ·	·

**Table 4-2. Example Relocatable Vector Table (for the M16C/62P)**

## 4.01 Defining Vector Tables

The BSP or application code should define fixed and relocatable vector tables. The vectors in the fixed vector table need not be used; indeed, some should not be used. The reset vector, for instance, should only direct program execution to the startup code. The other vectors in the fixed vector table should execute a dummy handler containing the return from interrupt instruction (REIT) if unused for other purposes.

The relocatable vector table must contain two entries; the others may be set to zero or assigned a dummy handler. The first entry that must be present is the μC/OS-II context switch handler, OSctxSw(), which should be placed on vector zero. The second is the μC/OS-II tick ISR handler, OSTickISR(), which should be placed on the vector associated with the timer that generates the μC/OS-II time tick.

### 4.01.01 IAR Vector Table

For the IAR project ports, the vector tables are defined in the assembly file *app\_vect.s34*, included as part of the application code. Listing 4-1 and 4-2 present the fixed and relocatable vector tables, respectively.

```

MODULE ?vectors1

EXTERN __program_start          ; Note 1
EXTERN UndefHandler            ; Note 2
EXTERN OverflowHandler
EXTERN BreakHandler
EXTERN AddressMatchHandler
EXTERN SingleStepHandler
EXTERN WatchdogHandler
EXTERN DBCHandler
EXTERN NMHandler

COMMON INTVEC1:NOROOT

DC32 UndefHandler
DC32 OverflowHandler
DC32 BreakHandler
DC32 AddressMatchHandler
DC32 SingleStepHandler
DC32 WatchdogHandler
DC32 DBCHandler
DC32 NMHandler
DC32 __program_start           ; Reset vector

ENDMOD
```

**Listing 4-1. *app\_vect.s34*: Fixed Vector Table, IAR Port**

**Listing 4-1, Note 1:** This is externed from the BSP's *cstartup.s34* code.

**Listing 4-1, Note 2:** The dummy handlers are defined from a different module in the same file. These dummy handlers just execute the REIT instruction.

```

MODULE ?vectors2

EXTERN OSCtxSw
EXTERN OSTickISR

PUBLIC RelocatableVectTbl          ; Note 1

RSEG INTVEC:NOROOT

RelocatableVectTbl:
  ORG 0
  DC32 OSCtxSw                      ; Note 2: Vector 0: BRK
  DC32 0                            ; Vector 1: Reserved
  DC32 0                            ; Vector 2: Reserved
  DC32 0                            ; Vector 3: Reserved
  DC32 0                            ; Vector 4: INT3
  DC32 0                            ; Vector 5: Timer B5
  DC32 0                            ; Vector 6: Timer B4, UART1 Bus Collision
  DC32 0                            ; Vector 7: Timer B3, UART0 Bus Collision
  DC32 0                            ; Vector 8: SI/O4, INT5
  DC32 0                            ; Vector 9: SI/O3, INT4
  DC32 0                            ; Vector 10: UART2 Bus Collision Detect
  DC32 0                            ; Vector 11: DMA0
  DC32 0                            ; Vector 12: DMA1
  DC32 0                            ; Vector 13: Key Input Interrupt
  DC32 0                            ; Vector 14: A/D
  DC32 0                            ; Vector 15: UART2 Transmit, NACK2
  DC32 0                            ; Vector 16: UART2 Receive, ACK2
  DC32 0                            ; Vector 17: UART0 Transmit, NACK0
  DC32 0                            ; Vector 18: UART0 Receive, ACK0
  DC32 0                            ; Vector 19: UART1 Transmit, NACK1
  DC32 0                            ; Vector 20: UART1 Receive, ACK1
  DC32 0                            ; Vector 21: Timer A0
  DC32 0                            ; Vector 22: Timer A1
  DC32 0                            ; Vector 23: Timer A2
  DC32 0                            ; Vector 24: Timer A3
  DC32 0                            ; Vector 25: Timer A4
  DC32 OSTickISR                    ; Note 3: Vector 26: Timer B0
  DC32 0                            ; Vector 27: Timer B1
  DC32 0                            ; Vector 28: Timer B2
  DC32 0                            ; Vector 29:
  DC32 0                            ; Vector 30:
  DC32 0                            ; Vector 31:

ENDMOD

```

**Listing 4-2. *app\_vect.s34*: Relocatable Vector Table, IAR Port**

**Listing 4-2, Note 1:** This will be used in *cstartup.s34* to initialize the INTB register.

**Listing 4-2, Note 2:** *OSCtxSw()* is placed on IRQ vector 0.

**Listing 4-2, Note 3:** The BSP (Board Support Package) uses timer B0 to generate the μC/OS-II tick interrupt. Consequently, *OSTickISR()* is placed on IRQ vector 26.

## 4.01.02 HEW Vector Table

For the HEW project ports, the vector tables are defined in the assembly include file *\_linker.inc*, included as part of the BSP code. Listing 4-3 and 4-4 present the fixed and relocatable vector tables, respectively.

```
UDI:      .lword  dummy_int          ; Note 1
OVER_FLOW: .lword  dummy_int
BRKI:     .lword  dummy_int
ADDRESS_MATCH: .lword  dummy_int
SINGLE_STEP: .lword  dummy_int
WDT:      .lword  dummy_int
DBC:      .lword  dummy_int
NMI:      .lword  dummy_int
RESET:    .lword  start            ; Note 2
```

**Listing 4-3. *\_linker.inc*: Fixed Vector Table, HEW Port**

**Listing 4-3, Note 1:** The dummy handler just executes the `REIT` instruction.

**Listing 4-3, Note 2:** This is defined in the BSP's *\_cstartup.a30* code.

```

.section      vector

.glob        _OSCtxSw
.glob        _OSTickISR

.org         VECTOR_ADR      ; Note 1

.LWORD      _OSCtxSw        ; Note 2: Vector  0: BRK
.LWORD      0                ;           Vector  1: Reserved
.LWORD      0                ;           Vector  2: Reserved
.LWORD      0                ;           Vector  3: Reserved
.LWORD      0                ;           Vector  4: INT3
.LWORD      0                ;           Vector  5: Timer B5
.LWORD      0                ;           Vector  6: Timer B4, UART1 Bus Collision
.LWORD      0                ;           Vector  7: Timer B3, UART0 Bus Collision
.LWORD      0                ;           Vector  8: SI/O4, INT5
.LWORD      0                ;           Vector  9: SI/O3, INT4
.LWORD      0                ;           Vector 10: UART2 Bus Collision Detect
.LWORD      0                ;           Vector 11: DMA0
.LWORD      0                ;           Vector 12: DMA1
.LWORD      0                ;           Vector 13: Key Input Interrupt
.LWORD      0                ;           Vector 14: A/D
.LWORD      0                ;           Vector 15: UART2 Transmit, NACK2
.LWORD      0                ;           Vector 16: UART2 Receive,  ACK2
.LWORD      0                ;           Vector 17: UART0 Transmit, NACK0
.LWORD      0                ;           Vector 18: UART0 Receive,  ACK0
.LWORD      0                ;           Vector 19: UART1 Transmit, NACK1
.LWORD      0                ;           Vector 20: UART1 Receive,  ACK1
.LWORD      0                ;           Vector 21: Timer A0
.LWORD      0                ;           Vector 22: Timer A1
.LWORD      0                ;           Vector 23: Timer A2
.LWORD      0                ;           Vector 24: Timer A3
.LWORD      0                ;           Vector 25: Timer A4
.LWORD      _OSTickISR      ; Note 3: Vector 26: Timer B0
.LWORD      0                ;           Vector 27: Timer B1
.LWORD      0                ;           Vector 28: Timer B2
.LWORD      0                ;           Vector 29:
.LWORD      0                ;           Vector 30:
.LWORD      0                ;           Vector 31:

```

**Listing 4-4. *\_linker.inc*: Relocatable Vector Table, HEW Port**

**Listing 4-4, Note 1:** This will be used in *\_cstartup.a30* to initialize the INTB register.

**Listing 4-4, Note 2:** *OSCtxSw()* is placed on IRQ vector 0. In HEW, C variables referred to in assembly files must be preceded by an underscore.

**Listing 4-4, Note 3:** The BSP (Board Support Package) uses timer B0 to generate the μC/OS-II tick interrupt. Consequently, *OSTickISR()* is placed on IRQ vector 26.

## 4.02 Example Interrupt Service Routine

The interrupt controller for the M16C/R8C is naturally a vectored controller; consequently, a small amount of assembly-language code must be written for each interrupt vector (in either the relocatable or fixed vector tables) that will be used. This will be the same code for each interrupt vector.

```

ExampleISR:

    PUSHM      R0,R1,R2,R3,A0,A1,SB,FB      ; Note 1: Save current task's registers

    INC.B      OSIntNesting                  ; Note 2: OSIntNesting++
    CMP.B      #1,OSIntNesting              ; Note 3: if (OSIntNesting == 1) {
    JNE        OSTickISR1

    MOV.W      OSTCBCur, A0                  ;           OSTCBCur->OSTCBStkPtr = SP
    STC        ISP, [A0]                    ;           }

ExampleISR1:
    JSR        ExampleISRHandler          ; Note 4: ExampleISRHandler()

    JSR        OSIntExit                  ; Note 5: OSIntExit()

    POPM      R0,R1,R2,R3,A0,A1,SB,FB      ; Note 6: Restore current task's registers

    REIT
  
```

**Listing 4-5. Example ISR**

**Listing 4-5, Note 1:** The current task's registers are saved.

**Listing 4-5, Note 2:** The interrupt nesting level is incrementing.

**Listing 4-5, Note 3:** If a task was interrupted, then the stack pointer is saved..

**Listing 4-5, Note 4:** ISR performs whatever function it should. This example ISR calls a function that could be written in C, `ExampleISRHandler()`.

**Listing 4-5, Note 5:** `OSIntExit()` is called to determine if a task with a higher priority than the one interrupted exists. If one does, then `OSIntExit()` never returns.

**Listing 4-5, Note 6:** The current task's registers are restored.

## Licensing

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## References

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